71. (New) The system according to claim 67, wherein the bidirectional data bus is a single 16 bit bus, supports 64 data buffers, and operates at 800 MHz.

REMARKS

Claims 5, 6, 29, 31-35, 38-45, 48-53, and 56 are amended, no claims are canceled, and claims 57-71 are added; as a result, claims 5-9, and 29-71 are now pending in this application.

Claim Objections

Claims 5-8 and 29-56 for objected to for not giving a clear depiction of the buffering which is being performed in the invention. Applicant amends the above claims as suggested by the Examiner. Accordingly, the above amendments are made to overcome the objections and not made for purposes of patentablility over any prior art. Thus, these amendments should not affect the scope of any equivalents that such elements are entitled. Withdrawal of the claim objections is requested.

Double Patenting Rejection

Claims 5-8 and 29-56 were provisionally rejected under the judicially created doctrine of obviousness-type double patenting over claims 1-4, 26-28, and 32-57 of co-pending U.S. Application No. 08/886,753. Applicant notes the rejection and will consider a Terminal Disclaimer upon an indication of allowable subject matter in the present application.

Reservation of the Right to Swear Behind References

Applicant maintains its right to swear behind any references which are cited in a rejection under 35 U.S.C. §§102(a), 102(e), 103/102(a), and 103/102(e). Statements distinguishing the claimed subject matter over the cited references are not to be interpreted as admissions that the references are prior art.

§103 Rejection of the Claims

Claims 5-8 and 29-56 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Katayama et al. (U.S. Patent No. 5,875,452) in view of Sakakibara et al. (U.S. Patent No. 5,617,575).

Applicant respectfully notes that Katayama does not teach or suggest all of elements recited in claim 5. For example, Figures 1 and 9 of Katayama do not show "a plurality M of memory devices wherein each memory device contains a data in and a data out buffer, a column decoder and a row decoder; ...a command buffer ...and a data buffer [emphasis added]." The Office Action states "a plurality of memory devices (note the use of two exemplary DRAM devices 22)". Figure 2 of Katayama does not show that each memory device 22 has a data in and data out buffer as recited in claim 5. Katayama merely shows write buffer 52 and read buffer 54 for all of the memory devices 22. More specifically, it is believed that Katayama does not teach a plurality of memory devices having a buffer, column decoder and row decoder.

Moreover, if Katayama's read and write buffers 52, 54 are read as the data in and the data out buffer as recited in claim 1, then Katayama does not have a data buffer that is connected to a plurality of memory devices as recited in claim 5.

Accordingly, Katayama does not teach all of the elements of claim 5. Applicant respectfully submits that claim 5 patentably distinguishes over Katayama under 35 U.S.C. §103.

The Office Action further relies on St. Regis Paper Co. v. Bemis Co., 193 USPQ 8 (7th Cir. 1977) for not lending patentable weight to each of the memory devices having a data in and a data out buffer. Applicant cannot agree with this assertion. Specifically, the feature of each memory device containing a data in and a data out buffer, a column decoder and a row decoder was added to the claims to clarify that these components are internal to each memory device and that within the memory system a command buffer and a data buffer corresponding to a plurality of memory devices are in addition to the internal components of each memory device because these features do, in fact, lend patentable weight. For example, the corresponding command buffer and data buffer result in an effect greater than the sum of the several effects taken separately. As illustrated by memory system 100 comprising N command and address buffers 131, N data buffers and N*M DRAMS (See Fig. 1 of the present application). Each command and address buffer drives the latched command and address information to its corresponding

plurality of memory devices. In this manner, the load on the C/A bus is reduced from N*M devices to only N devices. Additionally, the load on data bus 120 is reduced from N*M devices to only N devices. As a result the effects of the data in and data out buffer of each of the plurality of memory devices, in combination with the command buffer and the data buffer within the memory system are more than the sum of the single effects of the internal components of each of the plurality of memory devices. The addition of a command buffer coupled between a corresponding plurality of memory devices and a unidirectional command and address bus and a data buffer coupled between the corresponding plurality of memory devices and a bidirectional data bus results in a memory system which uses a single 16-bit data bus which can be operated at 800 MHZ and which supports 64 devices. In sum, the present invention as defined by the claims is not obvious under §103. And is certainly not analogous to the St. Regis court's interpretation of redundancy which found merely adding layers to a paper bag was obvious.

The Office Action goes on to state that ""the plurality of sense amps 28 (note column 17, lines 12-14) in Figure 2 would have required multiple dedicated read and write buffers 54 and 52." However, the undersigned can find no reference at column 17, lines 12-14 of such a teaching as contained in the claims. As stated above, it is believed that Katayama does not teach a plurality of memory devices having a buffer, column decoder and row decoder. Applicant respectfully requests further clarification as to where this teaching is found in Katayama.

It should further be noted that the office action admits that

> While Katayama et al. teaches most of the features of the invention as described above, there is no specific teaching of a shared command buffer and a shared data buffer, where these buffers are shared among plural memory banks.

The office action goes on to state that

> However, shared buffers were well known in the prior art. In fact, as stated in the previous advisory action, most of the present claims are written so broadly that they would have been taught by the use of an instruction buffer and a data buffer at processor (12) of the Katayama et al. system.
>
> Although Katayama et al. did not discuss the structure of the processor (12), it is noted that most processors on the market at the time of the invention utilized integral data buffers and instruction buffers at the respective bus interfaces.

Applicant respectfully traverses this assertion as a form of official notice and requests a reference to support the assertion or withdrawal of the assertion according to MPEP 2144.03. In the alternative, Applicant requests that the examiner provide a sworn affidavit as to his beliefs on this assertion. Moreover, reference is made to claim 5, which states "a command buffer connected between the command and address bus and the plurality of memory devices, ...and a data buffer connected between the plurality of memory devices and the bidirectional data bus ..." Accordingly, claim 5 recites structure which is patentably distinct over the alleged prior art processors having buffers, which buffers would be positioned between the processor and the bus.

Referring now to Sakakibara, applicant respectfully disagrees with the examiner's interpretation of Sakakibara's multiple processor computer system. First, the storage control unit 9 is not a "shared command buffer unit" as asserted in the office action. Sakakibara's storage control unit 9 is a memory controller, which receives memory request signals and memory access priority signals from multiple processors VP0-VP3. Therefore, the storage control unit may be read as analogous to the memory controller as recited in claim 5. Consequently, Sakakibara does not teach or even suggest a command buffer as recited in claim 5.

Further in contrast to claim 1, Sakakibara does not position its storage control unit 9 between its bus (paths 10-14) and the main memory storage 14. As discussed in greater detail above, claim 5 connects its command and data buffers between the plurality of memory devices and the data bus to achieve improved memory capacity, size and speed, while not having to increase the number of bus paths or reduce the operating frequency. Sakakibara does not address any of the problems of using conventional methods to increase memory capacity. Instead, Sakakibara merely addresses operation of a multiple processor system.

Still further in contrast to claim 5, Sakakibara does not teach "a data in and a data out buffer" internally within each of its plurality of memory devices 15-18. Consequently, Katayama and Sakakibara, either alone or in combination, do not teach or even suggest all of the features recited in claim 5, for example, a data in and a data out buffer.

Referring now to a combination of Katayama and Sakakibara, there is no expectation of success in combining these documents absent the teachings of the present disclosure. Claim 5 recites a novel architecture which is not taught by either Katayama or Sakakibara. Moreover, neither Katayama nor Sakakibara are directed to the problem of increasing memory capacity

while not increasing the number of traces laid on an integrated circuit or degrading memory access times by increasing the load on a command\address bus. Accordingly, one of ordinary skill in the art would not look to Katayama and Sakakibara for teachings to solve these problems and arrive at the present invention as defined by the claims.

Based at least on the reasons stated above, it is respectfully submitted that claim 5 is allowable over Katayama and Sakakibara under 35 U.S.C. §103. Claims 6-8 and 59-62 depend from claim 5 and are also believed allowable therewith.

Claims 34-37, 44-47, 52-55 are believed to be allowable for at least substantially similar reasons as those stated above with regard to claim 5. However, it should be noted that claims 34, 44 and 52 do not include the feature of the data buffer being shared by the plurality of memory devices as recited in claim 5. Accordingly, any above discussion of this feature is not applicatable to claims 34, 44 and 52.

New claims

Claims 57-71 are added. It is believed that these claims are supported by the originally-filed disclosure. Accordingly, no new matter is proposed. Consideration of claims 57-71 is respectfully requested.

CONCLUSION

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney at (612) 349-9587 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

KEVIN J. RYAN

By their Representatives,

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. Box 2938
Minneapolis, MN 55402
(612) 349-9587

Date 6/15/01 By _____
Timothy B. Clise
Reg. No. 40,957

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner of Patents, Washington, D.C. 20231, on this 15 day of June, 2001.

Tina Pugh
Name

_____
Signature